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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,731	03/31/2000	Hans Eberle	1004-4254	1939

22120 7590 03/28/2003

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EXAMINER	
NGUYEN, PHUOC H	
ART UNIT	PAPER NUMBER
2143	6

DATE MAILED: 03/28/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/540,731	Applicant(s) EBERLE ET AL.	
	Examiner Phuoc H. Nguyen	Art Unit 2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2,4,5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1,3,5-17 rejected under 35 U.S.C. 102(b) as being anticipated by Levinson U.S. Patent 5,566,171.

3. Referring to claim 1, Levinson reference discloses a plurality of initiator nodes coupled to send packets, into the network (Figures 9,10, and 11); a plurality of target nodes coupled to receive packets sent into the network (Figures 9,10, and 11); and a plurality of pipeline stages for transmitting data across the network, each pipeline stage consuming a predetermined time period, thereby providing for a predetermined time period for transmission for each packet successfully sent between one of the initiator nodes and one of the target nodes (Abstract; and col. 36-47).

4. Referring to claim 3, Levinson reference discloses the pipeline stages include an arbitration stage, a transfer stage, an acknowledge stage, the stages being in a fixed time relation to each other (col. 5, lines 50-59).

5. Referring to claim 5, Levinson reference discloses a check stage in which an initiator node checks if transmission of a sent packet was successful (Fig. 7c; col. 10, lines 4-22); and col. 16, lines 61 through col. 17, lines 10).

6. Referring to claim 6, Levinson reference discloses arbitration logic coupled to the initiator nodes, the pipelined network, and the target nodes, the initiator nodes supplying requests to the arbitration logic for transmission of respective packets to respective target nodes during respective arbitration stages, the arbitration logic responsive to the initiator node requests to schedule packet transmission across the network (col. 5, lines 50-59).

7. Referring to claim 7, Levinson reference discloses a particular transfer, the arbitration logic is coupled to receive an indication from a particular target node for the particular transfer as to whether the particular transfer can be supported in the particular target node (col. 5, lines 50-59).

8. Referring to claim 8, Levinson reference discloses during the transfer stage the packet supplied by the initiator traverses the network (Fig. 9a, and fig. 10).

9. Referring to claim 9, Levinson reference discloses during the acknowledge stage, an acknowledge packet is returned by the target node to the initiator node (Fig. 7d, and col. 10, lines 45-52).

10. Referring to claim 10, Levinson reference discloses the acknowledge packet is checked by the initiator during the check stage (Fig. 7c, and col. 14-21).

11. Referring to claim 11, Levinson reference discloses the check stage is fixed in time in relation to the arbitration stage, thereby allowing the initiator node to check for successful completion of sending the packet a fixed time after the arbitration stage (col. 10, lines 4-22; and col. 16, lines 61 through col. 17, lines 10).

12. Referring to claim 12, Levinson reference discloses the transfer stage includes multiple pipeline stages to transmit the transfer packet across the network (Fig. 10).

13. Referring to claim 13, Levinson reference discloses the acknowledge stage includes multiple stages to transmit the acknowledge packet across the network (Fig. 12; and col. 14, lines 39-55).

14. Referring to claim 14, Levinson reference discloses the number of bytes transferred per request during the transfer stage is fixed (col. 5, lines 60 through col. 6, lines 16).

15. Referring to claim 15, Levinson reference discloses outstanding transactions across the pipelined network are delivered in order (col. 14, lines 40-44).

16. Referring to claim 16, Levinson reference discloses a switch coupling the nodes on the pipelined network (Fig. 17).

17. Referring to claim 17, Levinson reference discloses the pipelined network comprises a plurality of cascaded switches (Fig. 11, and fig. 12).

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 2,4, 31-36 rejected under 35 U.S.C. 103(a) as being unpatentable over Levinson in view of Manapat et al. U.S. Patent 6,327,175.

20. Referring to claims 2, and 4, Levinson reference disclose a plurality of pipeline stages for transmitting data across the network; however, Levinson fails to disclose the pipelined network

is synchronous in that boundaries of all the pipeline stages are aligned, and pipeline stages having equal length.

Manapat discloses that the pipelined network is synchronous in that boundaries of all the pipeline stages are aligned, and pipeline stages having equal length (col. 6, lines 44-50).

It would have been obvious to one of the ordinary skill in the art at the time of the invention was made to incorporate Manapat's teaching into Levinson's system to use a synchronous pipelined network, because the signals can easily control by a specific points in the clock cycle.

21. Referring to claim 31, Levinson reference discloses a plurality of processing nodes, each processing node including at least one processor (Figures 9,10, and 11); and pipelined switched network coupling the plurality of processing nodes, the pipelined network having a plurality of pipeline stages, the pipeline including at least an arbitration stage to obtain a path through the pipelined switched network, a transfer stage transferring data over the path and an acknowledge stage, each stage being of equal length (col. 5, lines 50-59; and col. 17, lines 36-47); however, Levinson fails to disclose a synchronous pipelined switched network coupling the plurality of processing nodes.

Manapat discloses a synchronous pipelined switched network (col. 6, lines 44-50).

It would have been obvious to one of the ordinary skill in the art at the time of the invention was made to incorporate Manapat's teaching into Levinson's system to use a synchronous pipelined network, because the signals can easily control by a specific points in the clock cycle.

22. Referring to claim 32, Levinson reference discloses the pipelined switched network comprises a first switching circuit coupling the plurality of processing nodes, the first switching circuit carrying information transmitted during the transfer stage (Fig. 1; and col. 3, lines 53 through col. 4, lines 3).

23. Referring to claim 33, Levinson reference discloses the pipelined switched network comprises a second switching circuit coupling the processing nodes, the second switching circuit being independent of the first switching circuit and wherein at least a portion of pipeline operations are carried over the second switching circuit simultaneous with operations for the transfer stage carried over the first switching circuit (Figures 11, 12; and col. 14, lines 29-55).

24. Referring to claim 34, Levinson reference discloses at least one of arbitration and acknowledge information for respective arbitration and acknowledge stages are transmitted over the second switching circuit (col. 13, lines 11-35).

25. Referring to claim 35, Levinson reference discloses the networked computer system further includes at least one storage node coupled to the plurality of processing nodes through the synchronous pipelined switched network (col. 1, lines 23-32).

26. Referring to claim 36, Levinson reference discloses the networked computer system further includes at least an input/output node coupled to the plurality of processing nodes through the synchronous pipelined switched network (Figures 1, and 8).

27. Claims 18-30 rejected under 35 U.S.C. 103(a) as being unpatentable over Levinson in view of Flanagin et al. U.S. Patent 4,674,082.

28. Referring to claim 18, Levinson reference discloses transmitting the information from an initiator node to a target node using a plurality of pipeline stages in the computer network, each

pipeline stage having a fixed forwarding delay (Abstract; col. 17, lines 36-47); however, Levinson fails to disclose that overlapping an operation in one pipeline stage with another operation in another pipeline stage.

Flanagin reference disclose the overlapping an operation in one pipeline stage with another operation in another pipeline stage (Fig. 10, fig. 11; and col. 5, lines 50-66).

It would have been obvious to one of the ordinary skill in the art at the time of the invention was made to incorporate Manapat's teaching into Levinson's system to use the overlapping technique to provide the interleaved effect. As a result, the pipeline stage can access alternate sections immediately without going to the waiting states.

29. Referring to claim 19, Levinson reference discloses requesting a path through the network from the initiator node to the target node during an arbitration stage from arbitration logic (col. 5, lines 50 through col. 6, lines 16); sending at least one data packet containing the information from the initiator node to the target node during one or more transfer stages (Fig. 16); and sending an acknowledge packet containing status of receipt of the data packet from the target to the initiator during one or more acknowledge pipeline stages (col. 8, lines 21-26).

30. Referring to claim 20, Levinson reference discloses the arbitration logic communicating with the target node to determine if the target node can accept a packet from the initiator node (col. 8, lines 21-26); and wherein during the arbitration stage, the arbitration logic provides a grant indication to the initiator node to indicate that the initiator node can transmit the packet during a subsequent transfer stage (col. 11, lines 58 though col. 12, lines 10; and col. 12, lines 24-39).

31. Referring to claim 21, Levinson reference discloses requesting a path through the network from the initiator node to the target node during an arbitration stage from arbitration logic; however, Levinson fails to disclose at least one of the arbitration stage, the transfer stage and the acknowledge stage are overlapped.

Manapat reference disclose the transfer stage and the acknowledge stage are overlapped (Fig. 10, fig. 11; and col. 5, lines 50-66).

It would have been obvious to one of the ordinary skill in the art at the time of the invention was made to incorporate Manapat's teaching into Levinson's system to overlapped the transfer stage and the acknowledge stage, because by overlapping the transfer stage and the acknowledge stage. This will provide the interleaved effect. As a result, the pipeline stage can access alternate sections immediately without going to the waiting states.

32. Referring to claim 22, Levinson reference discloses the pipelined network includes a first switching circuit coupling the initiator node and the target node, the first switching circuit carrying information transmitted during the transfer stage (Fig. 1; and col. 3, lines 53 through col. 4, lines 3).

33. Referring to claim 23, Levinson reference discloses the pipelined network includes a second switching circuit coupling the initiator node and the target node, the second switching circuit being independent of the first switching circuit and wherein information for at least a portion of pipeline operations are carried over the second switching circuit simultaneously with operations for the transfer stage carried over the first switching circuit (Fig. 11, fig. 12; and col. 14, lines 29-55).

34. Referring to claim 24, Levinson reference discloses information for the arbitration and acknowledge stages are carried over the second switching circuit during arbitration and acknowledge pipeline stages, respectively (col. 13, lines 11-35).

35. Referring to claim 25, Levinson reference discloses generating a schedule for traversing the pipeline stages of the network in the arbiter, the schedule determining for each slot on the pipeline, each slot being a length of a pipeline stage, which input port is connected to which output port (col. 5, lines 50-59).

36. Referring to claim 26, Levinson reference discloses each initiator node of a plurality of initiator nodes provides a request vector indicating one or more desired target nodes, to the arbitration logic, the request vectors for at least some of the initiator nodes including multiple target nodes and wherein the arbitration logic schedules a future pipeline slot to avoid conflicts, the arbitration logic globally scheduling use of the network (col. 11, lines 3-11).

37. Referring to claim 27, Levinson reference discloses the initiator node checking the acknowledge packet a fixed number of pipeline stages after sending the transfer packet, to determine whether transmission of the information was successful (col. 10, lines 4-22; and col. 16, lines 61 though col. 17, lines 10).

38. Referring to claim 28, Levinson reference discloses scheduling usage of the network using an arbiter in response to requests from initiator nodes to allocate each stage of the pipeline so as to avoid conflicts for network resources (col. 10, lines 3-11).

39. Referring to claim 29, Levinson reference discloses the scheduling includes accounting for prescheduled requests, the prescheduled requests requesting periodic slots on the network (col. 10, lines 3-11).

40. Referring to claim 30, Levinson reference discloses sending all information across the network in order (col. 14, lines 40-44; and col. 18, lines 48-56).

Conclusion

41. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Madonna U.S. Patent 5,544,163

Holt et al. U.S. Patent 5,790,545

Chiang U.S. Patent 6,336,156

Chao U.S. Patent 6,487,213

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phuoc H. Nguyen whose telephone number is 703-305-5315. The examiner can normally be reached on Mon -Thu (7AM-4:30PM) and off every other Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A Wiley can be reached on 703-308-5221. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-7239 for regular communications and 703-746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Phuoc H. Nguyen
Examiner
Art Unit 2143

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February 27, 2003

DAVID WILEY
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100